

VLSI Design

Lecture 15: Memory Elements

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Adapted, with modifications, from lecture notes
prepared by the author (from Prentice Hall PTR)

Topics

- Memory elements.
- Basics of sequential machines.

Memory elements

- Store a value as controlled by clock.
- May have load, clear, set signals, etc.
- In CMOS, memory is created by:
 - ❖ capacitance (dynamic);
 - ❖ feedback (static).

Variations in memory elements

- Form of required clock signal.
- How behavior of data input around clock affects the stored value.
- When the stored value is presented to the output.
- Whether there is ever a combinational path from input to output.

Memory element terminology

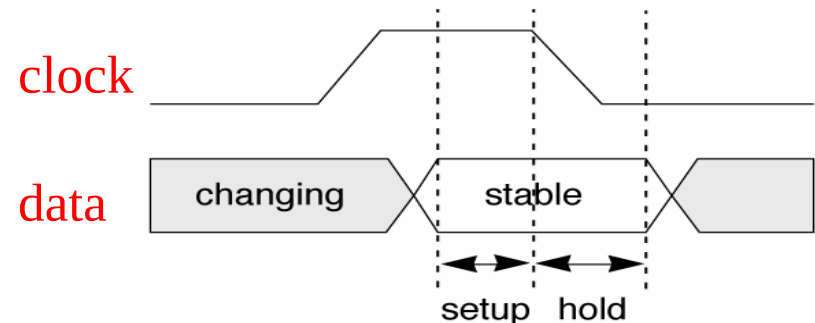
- Latch: **transparent** when internal memory is being set from input.
- Flip-flop: **not transparent**—reading input and changing output are separate events.

Clock terminology

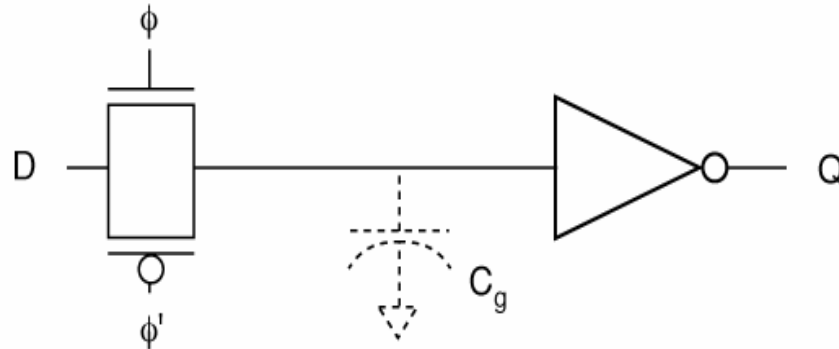
- Clock edge: rising or falling transition.
- Duty cycle: fraction of clock period for which clock is active (e.g., for active-low clock, fraction of time clock is 0).

Memory element parameters

- Setup time: time before clock during which data input must be stable (normally, the time required for the input to affect the storage node).
- Hold time: time after clock event for which data input must remain stable (delay from clock to disabling the storage node).
- Setup and hold times, along with the combinational delay, determine the speed of the system.
- Figure shows the parameters, assuming that the falling edge is the active edge.

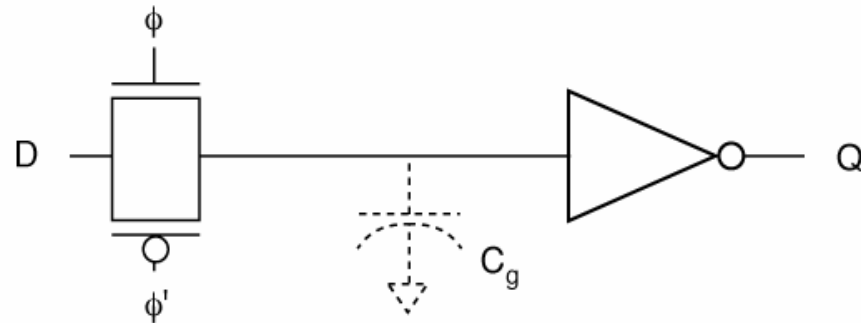


Dynamic latch



- Stores charge on inverter gate capacitance.
 - ❖ Storage capacitance comes primarily from inverter gate capacitance.
- Uses complementary transmission gate to ensure that storage node is always strongly driven.
- Latch is transparent when transmission gate is closed.

Latch operation

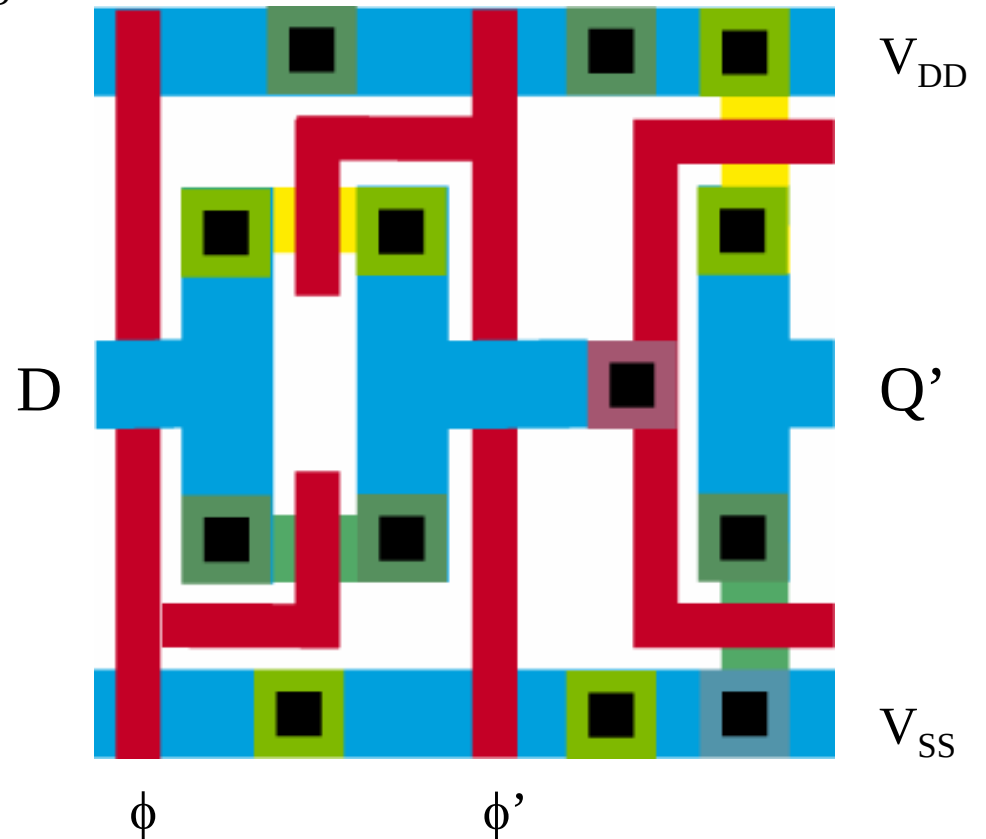
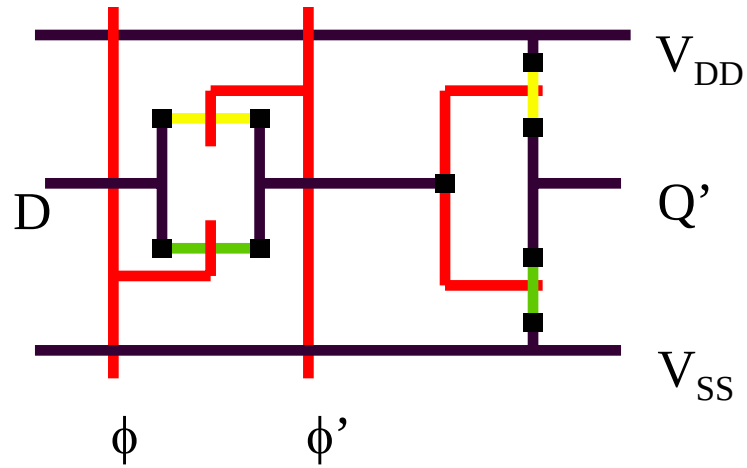


- $\phi = 0$: transmission gate is off, inverter output is determined by storage node.
- $\phi = 1$: transmission gate is on, inverter output follows D input.
- Setup and hold times determined by transmission gate: must ensure that value stored on transmission gate is solid.

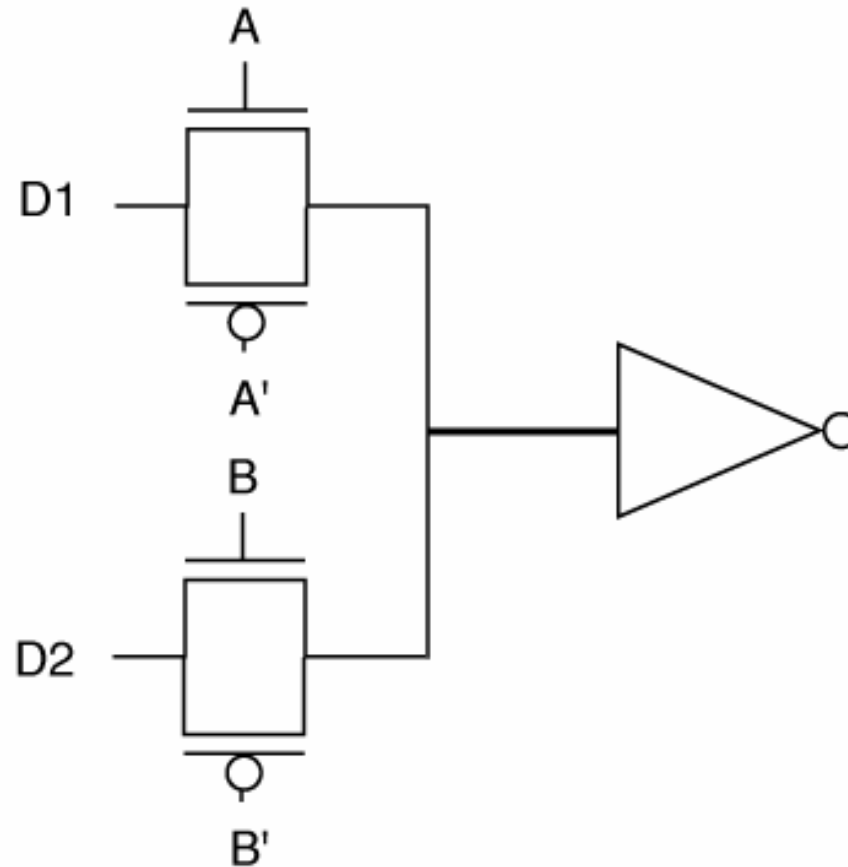
Stored charge leakage

- Stored charge leaks away due to reverse-bias leakage current, sub-threshold current, ...
- Stored value is good for about 1 ms (1 ns in modern processes!).
- Value must be rewritten to be valid.
- If not loaded every cycle, must ensure that latch is loaded often enough to keep data valid.

Stick diagram and Layout



Multiplexer dynamic latch

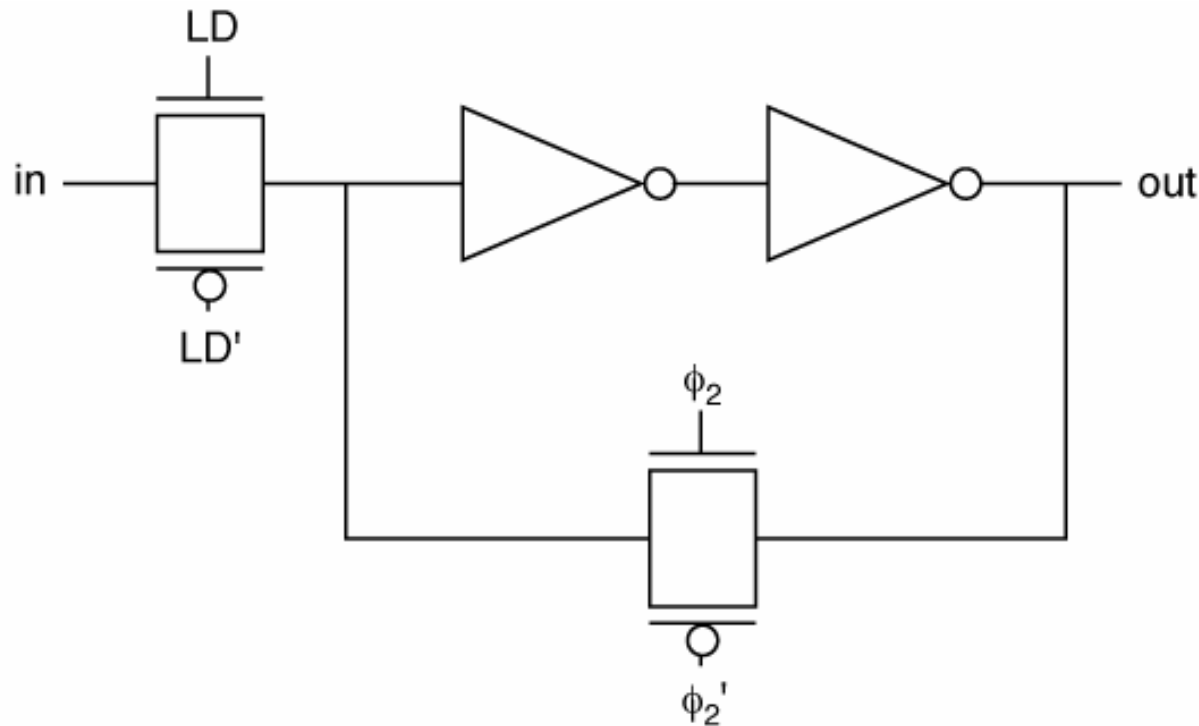


Non-dynamic latches

- Must use feedback to restore value.
- Some latches are static on one phase (pseudo-static): load on one phase, activate feedback on other phase.

Recirculating latch

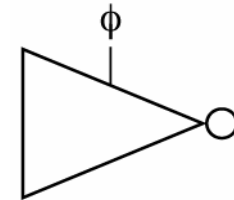
Static on one phase ($\phi_2=1 \Rightarrow$ Stored charge is preserved)



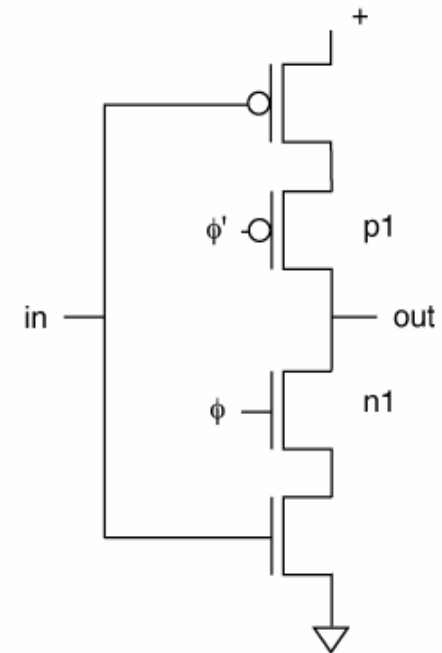
Clocked inverter

- Consists of an inverter merged with a transmission gate.
- $\phi = 0$: both clocked transistors are off, output is floating.
- $\phi = 1$: both clocked transistors are on, acts as an inverter to drive output.

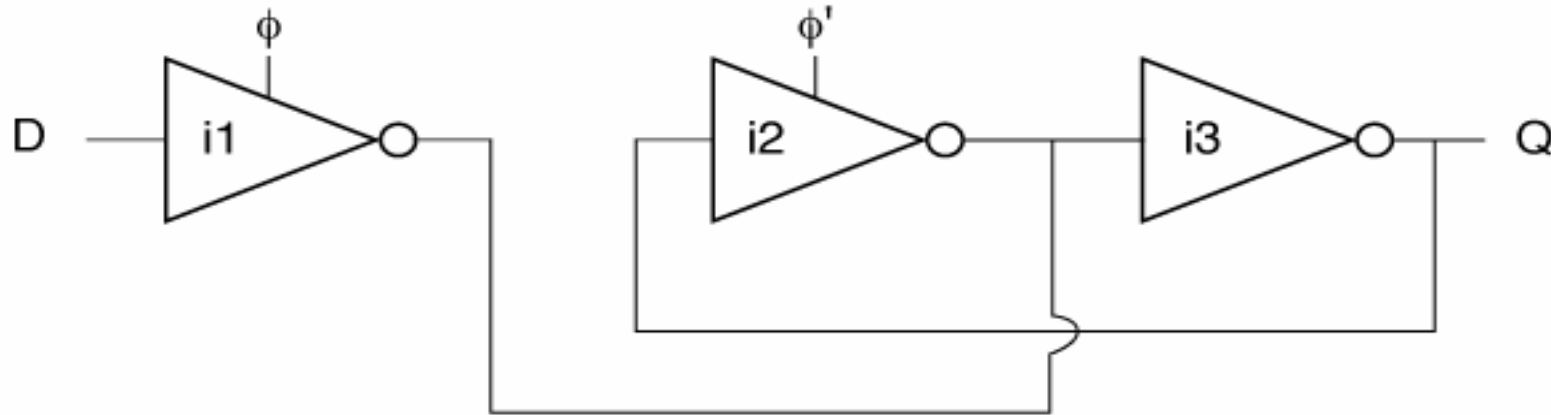
symbol



circuit



Clocked inverter latch



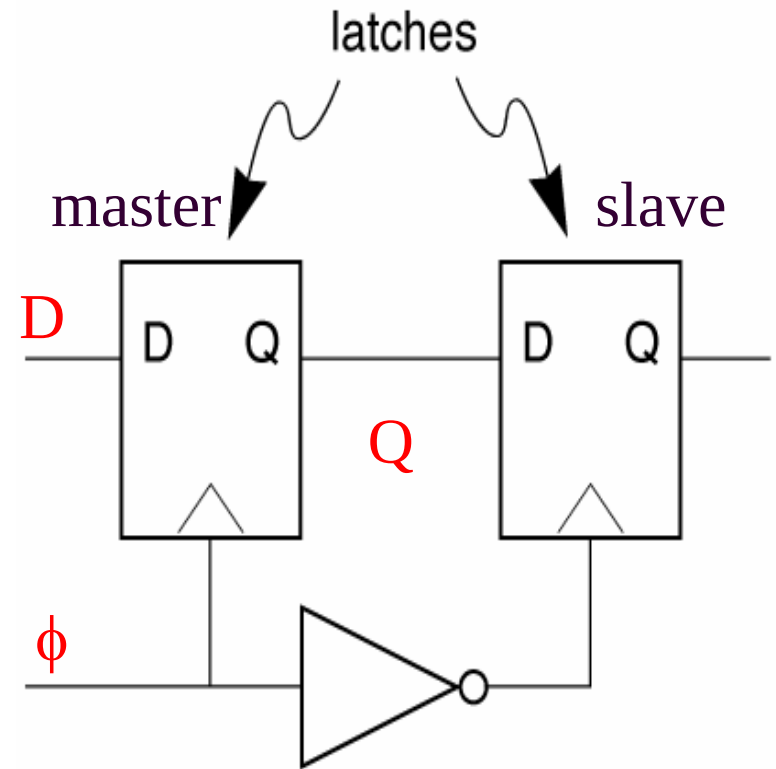
- $\phi = 0$: i1 is off, i2-i3 form feedback circuit.
- $\phi = 1$: i2 is off, breaking feedback; i1 is on, driving i3 and output.
- Latch is transparent when $\phi = 1$.

Flip-flops

- Not transparent: use multiple storage elements to isolate output from input.
- Major varieties:
 - ❖ master-slave;
 - ❖ edge-triggered.

Master-slave flip-flop

- $\phi = 0$: master latch is disabled; slave latch is enabled, but master latch output is stable, so output does not change.
- $\phi = 1$: master latch is enabled, loading value from input; slave latch is disabled, maintaining old output value.



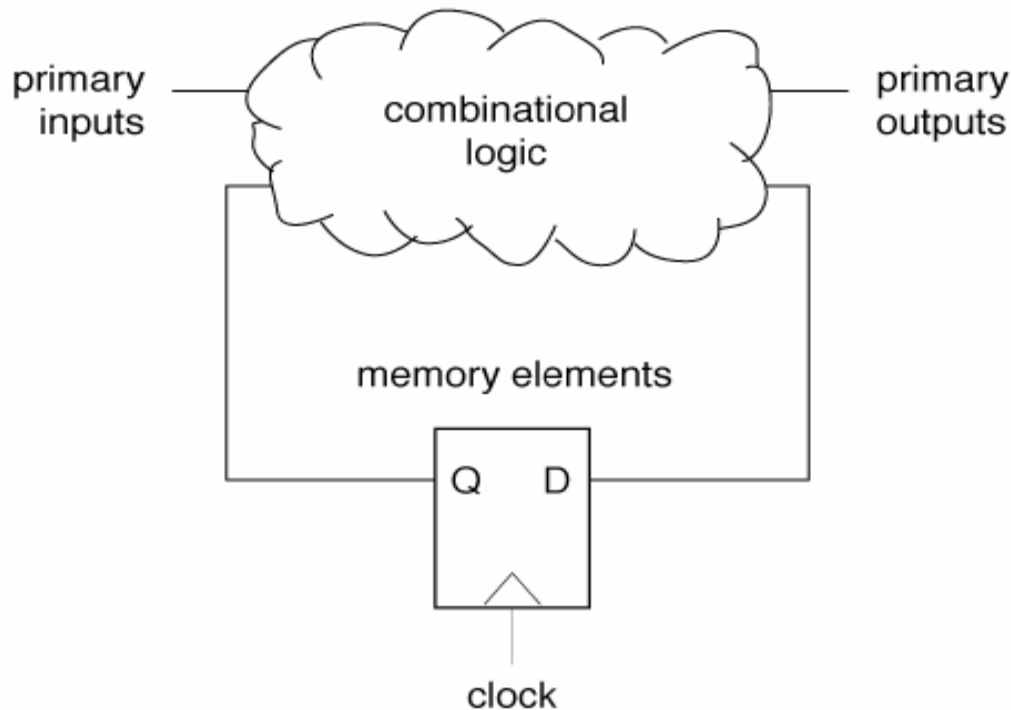
Sequential machines

- Use memory elements to make primary output values depend on state + primary inputs.
- Varieties:
 - ❖ Mealy: outputs function of present state, inputs;
 - ❖ Moore: outputs depend only on state.

Sequential machine definition

- Machine computes next state N , primary outputs O from current state S , primary inputs I .
- Next-state function:
 - ❖ $N = \delta(I, S)$.
- Output function (Mealy):
 - ❖ $O = \lambda(I, S)$.

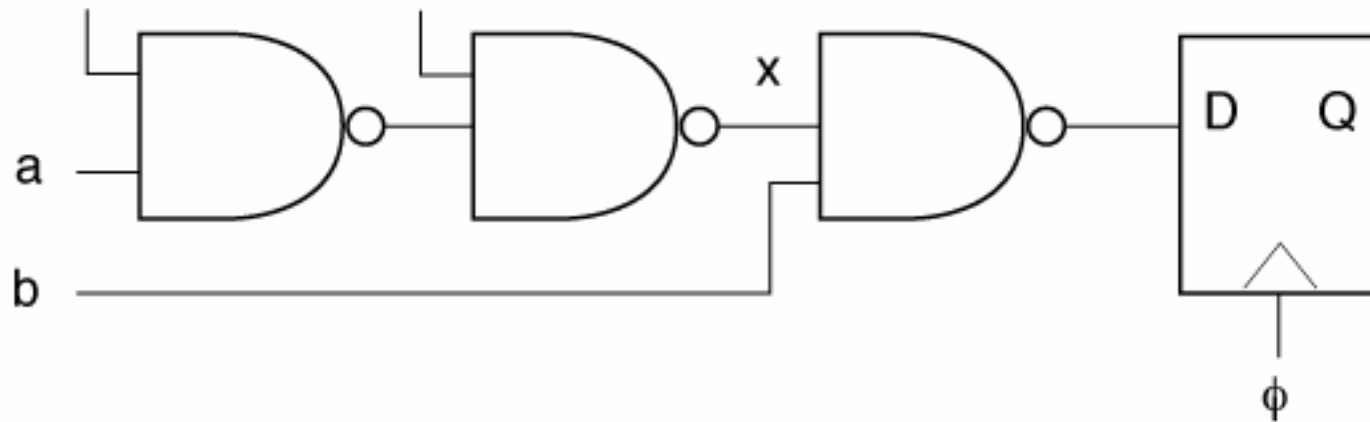
FSM structure and constraints



- No combinational cycles.
- All components must have bounded delay.

Signal skew

Machine data signals must obey setup and hold times: avoid signal skew.



Clock skew

Clock must arrive at all memory elements in time to load data.

